RECEIVED
CENTRAL FAX CENTER
MAR 2 7 2006

Specification Amendments

Please replace paragraph 007 with the following rewritten paragraph:

It is therefore an object of the invention to provide improved ~~the~~ etching profiles of gate electrode structures while reducing etching residues including triple-poly split gate configuration memory cells to thereby improve the yield and reliable operation of split gate flash memory devices, while overcoming other deficiencies and shortcomings of the prior art.

Please replace paragraph 014 with the following rewritten paragraph:

Shown in Figure 1A are gate structures 12A and 12B formed by conventional methods over silicon substrate (e.g., wafer) 10. It will be appreciated that doped regions (not shown) are included in the silicon substrate. For example, a gate oxide portion e.g., 14A, polysilicon gate electrode portion 14B, and interpoly insulating layer 14C are formed by conventional methods. For example, a stack of layers including a silicon oxide layer is thermally grown by conventional methods to conventional thicknesses, e.g., 50 Angstroms to 150 Angstroms followed by deposition of a polysilicon layer to a thickness between about 1000 Angstroms and 1500 Angstroms depending on design constraints~~, e.g., 1 micron~~ for CMOS technology. A dielectric insulating layer, also referred to as a first interpoly layer, preferably a high temperature oxide (HTO) layer, for example SiO_2, is thermally grown under dry or wet conditions over the polysilicon layer, for example to a thickness of between about 800 Angstroms and about 900 Angstroms. It will be appreciated that the first interpoly layer may be formed of an ONO (oxide-nitride-oxide) layer formed by known methods in the art.

PAGE 5/28 * RCVD AT 3/27/2006 9:30:04 AM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/38 * DNIS:2738300 * CSID:12485404035 * DURATION (mm-ss):05-06